after the initial supply.

Cont D2

3. (Twice Amended) The semiconductor integrated circuit according to claim 1, further comprising a voltage generator for generating an internal supply voltage in accordance with an external supply voltage, and wherein

said timing changing circuit changes an inactivation timing of the reset signal in accordance with the internal signal corresponding to said internal supply voltage.

A marked-up version of the amended claims is enclosed as required by 37 C.F.R. § 1.121.

REMARKS

Claims 1-13 are pending in this application. By this Amendment, claims 1-3 have merely been amended to more particularly point out and distinctly claim the invention. No new matter is presented. Accordingly, claims 1-13 are presented for consideration.

Applicant acknowledges and thanks the Examiner for indicating that claims 7-9 and 12-13 are allowed, and that claims 3-6, 10 and 11 would be allowable over the prior art if amended to be in independent form. However, Applicant respectfully submits that all of the presently pending claims recite allowable subject matter and therefore, placing claims 3-6, 10 and 11 into independent form is not necessary.

Claim 1 was objected to for certain informalities. By this amendment, it is respectfully submitted that the objection has been overcome. Therefore, the objection is requested to be withdrawn.

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Sawada (U.S. Patent No. 5,365,481). The Office Action asserted that Sawada discloses all the

elements of the claimed invention. However, the Applicant respectfully submits that claim 1 recites subject matter that is neither disclosed nor suggested in Sawada.

Claim 1 recites a semiconductor integrated circuit including a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit. The power-on resetting circuit also inactivates the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit. A timing changing circuit is provided for adjusting the predetermined period in accordance with an internal signal generated in the interior.

The Office Action took the position that Sawada discloses the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest such structure and, therefore, fails to provide the advantages that are provided by the present invention. For example, the timing changing circuit of the present invention adjusts the predetermined period, after which, the reset signal is inactivated in accordance with an internal signal generated in the interior.

As a result of this claimed configuration, the present invention prevents the reset signal from inactivating before the initialization of the internal circuit terminates and allows reliable initialization of the internal circuit. Additionally, the present invention enables adjustment of the time that the reset signal is inactivated without directly measuring the timing of the reset signal by utilizing the voltage generator transistor.

Sawada discloses a DRAM including a power-on reset circuit 17. Power-on reset circuit 17 receives power supply voltage V_{cc} and generates a first power-on reset signal POR1 which goes "H" during a predetermined period. A power-on reset circuit 18 generates a second power-on reset signal POR2 which goes "H" during a variable

period. Power-on reset circuit 19 receives POR1 and POR2 and generates a power-on reset signal for forcibly maintaining predetermined circuit units in the DRAM reset state.

In the present invention, a timing changing circuit adjusts a predetermined period before the reset signal is inactivated in accordance with an internal signal generated in the interior. However, Sawada only discloses a reset signal which changes the timing it inactivates in accordance to the external signal/RAS, which is an access signal. The external signal/RAS is a signal which the users supply to the semiconductor integrated circuit. This means that Sawada cannot achieve the result of the present invention which is that the inactivation timing which has deviated due to fluctuations in the manufacturing conditions of the semiconductor integrated circuit can be adjusted to a normal value, which is a benefit of the claimed invention. There is no disclosure or suggestion a power-on resetting circuit, which activates a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and inactivates the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit, as recited in claim 1. There is also no disclosure of suggestion of a timing changing circuit that adjusts the predetermined period in accordance with an internal signal generated in the interior, as also recited in claim 1.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claim 1, is not anticipated within the meaning of 35 U.S.C. § 102.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sawada in view of McKinney (U.S. Patent No. 5,389,843). In making this rejection, the Office Action took the position that Sawada discloses all the elements of the claimed invention with the exception of teaching that the timing changing circuit changes an

inactivation timing of the reset signal in accordance with the internal signal to be set at a predetermined logic level after the initial supply of a power supply. McKinney is cited for disclosing this limitation. However, the Applicant submits that claim 2 recites subject matter that is neither disclosed nor suggested by any combination of the prior art.

McKinney discloses a programmable variable length delay circuit. A signal to be delayed is input at STAGE 1. Delay element 10 provides a predetermined delay. Multiplexer 12 selects between the output of the delay element 10. The output of STAGE 1 is applied to the input of STAGE 2. STAGE 2 has delay element 20 and multiplexer 22.

In the present invention, a timing changing circuit changes an activation timing of the reset signal in accordance with the internal signal to be set at a predetermined logic level after the initial supply, as recited in claim 2.

The Office Action asserted that delay circuits are well known in the art and that it would have been obvious to incorporate the teachings of McKinney into Sawada to provide better adjustment of time delay of the power-on reset signal. However, firstly, simply changing the delay circuit in Sawada to a programmable delay circuit in McKinney does no achieve the same effect as in the invention in claim 2. Secondly, the motivation proffered in the Office Action for modifying Sawada in the manner suggested is neither taught nor suggested in either reference. Therefore, as discussed above, the combination of Sawada and McKinney fails to disclose or suggest the claimed invention.

Thus, it is respectfully submitted that the Applicant's invention, as set forth in claim 2, is not obvious within the meaning of 35 U.S.C. § 103(a).

Furthermore, as claim 2 depends from independent claim 1, Applicant submits that claim 2 also recites subject matter that is neither disclosed nor suggested by the prior art, for at least the reasons set forth above with respect to claim 1.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1 and 2 (claims 7-9, 12 and 13 already being allowed and claims 3-6, 10 and 11 being indicated as reciting allowable subject matter), and the prompt issuance of a Notice of Allowability are respectfully solicited.

If the application is not in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00042**.

Respectfully submitted,
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Enclosure: Marked-up Version of Amended Claims

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MARKED-UP VERSION OF AMENDED CLAIMS

Please amend claims 1-3 as follows:

1. (Three Times Amended) A semiconductor integrated circuit comprising:

a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and for inactivating the reset signal [to] after a predetermined period [after] following the initial supply to terminate an initialization of the internal circuit; and

a timing changing circuit for adjusting the predetermined period in accordance with an internal signal generated in the interior.

2. (Twice Amended) The semiconductor integrated circuit according to claim 1, wherein said timing changing circuit changes an inactivation timing of the reset signal in accordance with [a first set of signals] said internal signal to be set at a predetermined logic level after the initial supply.

3. (Twice Amended) The semiconductor integrated circuit according to claim 1, further comprising a voltage generator for generating an internal supply voltage in accordance with an external supply voltage, and wherein

said timing changing circuit changes an inactivation timing of the reset signal in accordance with the internal signal corresponding to said internal supply voltage.